WHAT IS CLAIMED IS:

1. A multi-chip package device with a heat sink, comprising:

a chip carrier for electrically connecting the semiconductor package device to an external device;

at least one first chip mounted on and electrically connected to a surface of the chip carrier;

at least one semiconductor package mounted on and electrically connected to the surface of the chip carrier; and

the heat sink mounted via an adhesion layer on a surface of the first chip and a surface of the semiconductor package that are opposite to surfaces of the first chip and the semiconductor package mounted on the chip carrier, wherein at least one hollow part extending through the heat sink is formed at an area of the heat sink free of contact with the first chip and the semiconductor package to release thermal stresses from the heat sink.

2. The multi-chip package device of claim 1, wherein the semiconductor package is a flip-chip ball grid array package.

3. The multi-chip package device of claim 1, wherein the first chip is a graphic chip.

4. The multi-chip package device of claim 1, wherein the first chip is a graphic processing unit.

5. The multi-chip package device of claim 1, wherein the semiconductor package is a Random Access Memory (RAM) unit.

6. The multi-chip package device of claim 1, wherein the first chip is mounted at the center of the chip carrier, and the semiconductor package is mounted at a position on the chip carrier corresponding to a corner of the heat sink.

7. The multi-chip package device of claim 1, wherein at least one pair of the semiconductor packages are mounted on the chip carrier, and the hollow part of the heat sink is located between the semiconductor packages.

8. The multi-chip package device of claim 1, wherein at least one symmetrical pair of the hollow parts are formed through the heat sink.

9. A fabrication method for a multi-chip package device with a heat sink, the method comprising steps of:

preparing a chip carrier and mounting at least one first chip and at least one semiconductor package on a surface of the chip carrier; and

mounting the heat sink via an adhesion layer on a surface of the first chip and a surface of the semiconductor package that are opposite to surfaces of the first chip and the semiconductor package mounted on the chip carrier, wherein at least one hollow part extending through the heat sink is formed at an area of the heat sink free of contact with the first chip and the semiconductor package to release thermal stress generated from the heat sink.

10. The fabrication method of claim 9, wherein the semiconductor package is a flip-chip ball grid array package.

11. The fabrication method of claim 9, wherein the first chip is a graphic chip.

12. The fabrication method of claim 9, wherein the first chip is a graphic processing unit.

13. The fabrication method of claim 9, wherein the semiconductor package is a Random Access Memory (RAM) unit.

14. The fabrication method of claim 9, wherein the first chip is mounted at the center of the chip carrier, and the semiconductor package is mounted at a position on the chip carrier corresponding to a corner of the heat sink.

15. The fabrication method of claim 9, wherein at least one pair of the semiconductor packages are mounted on the chip carrier, and the hollow part of the heat sink is located between the semiconductor packages.

16. The fabrication method of claim 9, wherein at least one symmetrical pair of the hollow parts are formed through the heat sink.

17. The fabrication method of claim 9, wherein the first chip is mounted on the chip carrier by flip-chip technology.

18. The fabrication method of claim 9, wherein the semiconductor package is mounted on the chip carrier by surface mount technology.